IDEC Chip Design Contest

Single Slope ADC-based Readout Circuits for Image Sensor

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Abstract

This paper describes the design and fabrication of a 10-bit, low noise, low power single slope analog-to-digital converter (SSADC) for high performance imaging applications that overcome these limitations by utilizing an advanced 180nm BCDMOS process. The proposed design features a highly flexible ramp generator with digitally controllable coarse/fine gain and offset, enabling optimization of the dynamic range and conversion speed for various operating conditions. Furthermore, it incorporates a low-noise, two-stage comparator to effectively reduce flicker noise and fixed-pattern noise through Correlated Double Sampling (CDS). This circuit includes achieving a 400-MHz effective ramp step rate from a 200-MHz clock via a double-edge triggering scheme to ensure high-speed conversion. The proposed operation was also verified through Cadence Virtuoso post-layout simulation.

Proposed Circuit System

◆ Principle of SSADC operation

- The proposed SSADC employs a column-parallel architecture composed of a ramp generator, a comparator.
- The input voltage is converted into time information by comparing the input level with a falling ramp signal until the crossing point
- Correlated double sampling (CDS) technique is performed during A/D conversion phase to suppress thermal noise and fixed-pattern noise (FPN).
- In this chip design, the pixel array and a N-bit counter is not included.

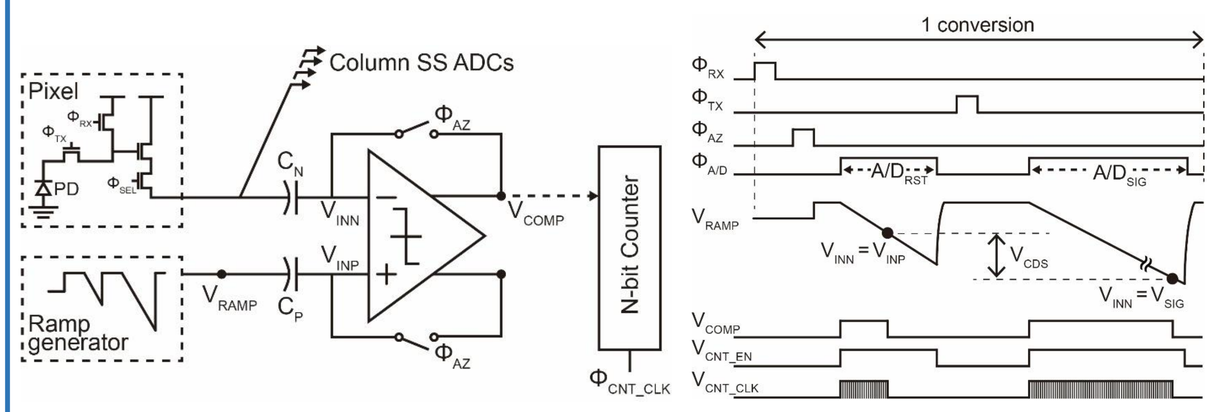

Fig. 1. Simplified column-parallel SSADC architecture (left) and operational timing diagram (right).

◆ Ramp generator design

- To generate a linearly falling ramp signal, the ramp generator consist of a current DAC, digital control logic, and a resistor bank.
- To achieve 10-bit resolution, a 32 × 48 CDAC array is employed. Due to nonlinear characteristics at the beginning and end of the ramp signal, the first and last 256 steps are excluded from conversion.
- Digitally controlled coarse gain, fine gain, and offset enable flexible adjustment of ramp swing, slope, and offset voltage for various operating conditions.

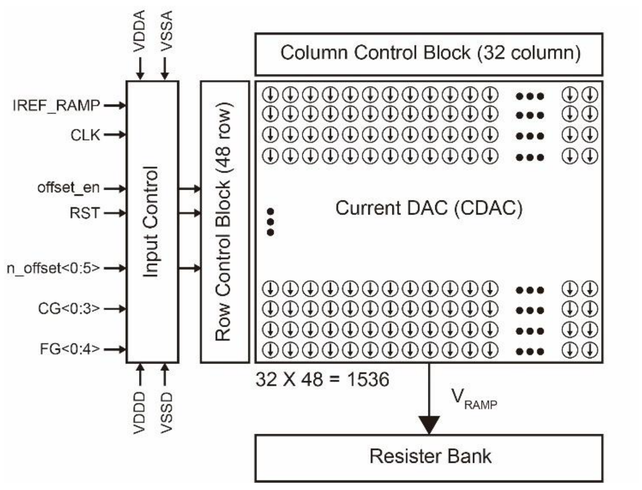

Fig. 2. Ramp generator block diagram.

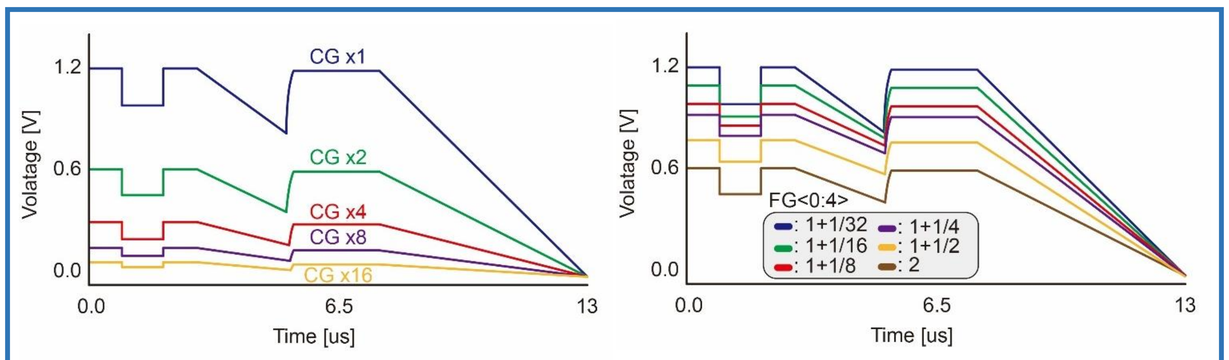

Fig. 3. Simulated ramp signal difference between CG and FG options.

◆ Comparator design

- CDS and auto-zeroing are adopted to suppress offset, flicker noise.
- OTA1 rejects common-mode ramp noise, and separate grounding for OTA1 and OTA2 is used to reduce switching noise.

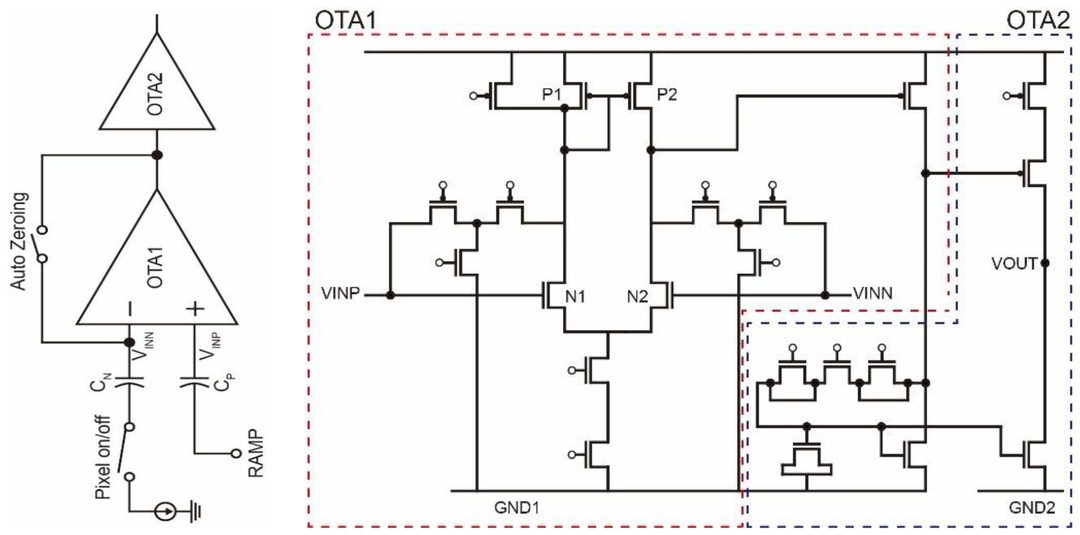

Fig. 4. Comparator block diagram (left) and OTA architecture (right).

◆ Simulation and measurement plan

- Post-layout simulation verified the correct operation of the ramp generator and comparator.
- The fabricated chip is currently in the PCB design progress. The evaluation plan includes ramp linearity, DNL/INL, SNR, SNDR, ENOB, and total power consumption.

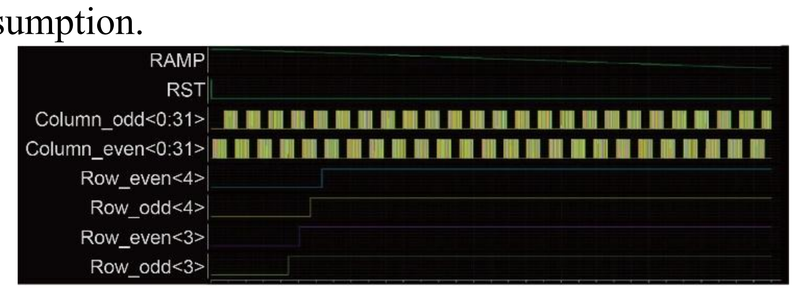

Fig. 5. Post-layout simulated control timing and ramp signal.

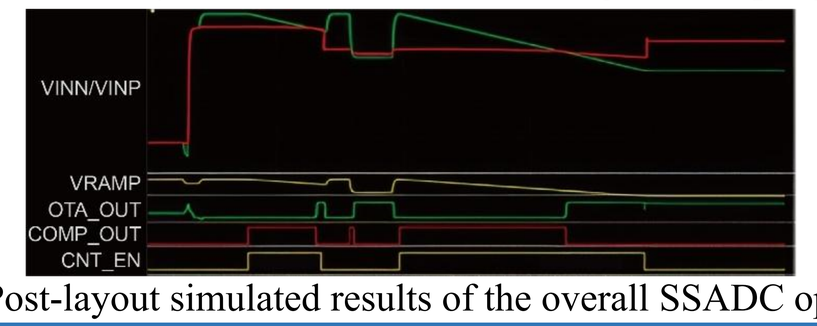

Fig. 6. Post-layout simulated results of the overall SSADC operation.

Conclusion

- A 10-bit, low-noise, low-power SSADC for column-parallel CMOS image sensors was designed and fabricated in a 180 nm BCDMOS process.
- The 4-bit coarse-gain and 5-bit fine-gain controls adjust the ramp swing range and slope to optimize the trade-off between dynamic range, SNR.
- Future work will verify the fabricated chip and extend the SSADC block with digital counter and logic for CMOS image sensor SoC integration.

Acknowledgement

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